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PATENT  
(5500-69000/TT4432)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/892,328  
Filed: June 26, 2001  
Inventor(s):  
Gerald D. Zuraski, Jr.

§ Examiner: Unknown  
§ Group/Art Unit: 2185  
§ Atty. Dkt. No: 5500-69000  
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on the date indicated below.

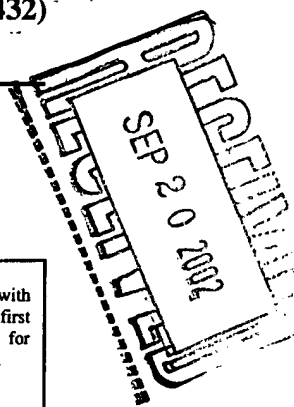
B. Noël Kivlin

Name of Registered Representative

Signature

Date

Title: Using Type Bits to Track  
Storage of ECC and  
Predecode Bits in a Level  
Two Cache



INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Washington, D.C. 20231



Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3. A copy of each reference listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

- a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);  
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;  
☒ before the mailing date of a first Office Action on the merits; or  
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.
- b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of \$180.00 is enclosed.

- c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of \$180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) \_\_\_\_\_, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

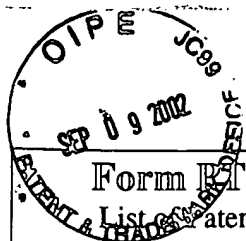
If any required fees are missing, the Commissioner is authorized to charge said fees to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5500-69000/BNK.

Respectfully submitted,

B. Noël Kivlin  
Reg. No. 33,929  
Attorney for Applicant(s)

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Date: 9/5/02



Form PTO-1449 (modified)  
List of Patents and Publications  
For Applicant's Information  
Disclosure Statement  
(Use several sheets if necessary)

ATTY. DKT. NO. 5500/69000

SERIAL NO. 09/892,328

APPLICANT: Gerald D. Zuraski, Jr.

GROUP: 2185

FILING DATE: June 26, 2001

## U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	5,951,671	9/14/99	Green			
	A2	5,828,895	10/27/98	Chan et al.			
	A3	5,819,067	10/6/93	Lynch			
	A4	5,752,264	5/12/98	Blake et al.			
	A5	5,751,981	5/12/98	Witt et al.			
	A6	5,748,978	5/5/98	Narayan et al.			
	A7	5,721,854	2/24/98	Ebcioğlu et al.			
	A8	5,689,672	11/18/97	Witt et al.			
	A9	5,265,004	11/23/93	Schultz et al.			
	A10	5,214,769	5/25/93	Uchida et al.			
	A11	4,942,519	7/17/90	Nakayama			
	A12	4,747,043	5/24/88	Rodman			
	A13	6,092,182	7/18/00	Mahalingaiah			

## FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A13	Advanced Micro Devices, Inc., <i>AMD Athlon™ Processor and AMD Duron™ Processor with Full-Speed On-Die L2 Cache: Enabling an Innovative Cache Architecture for Personal Computing</i> , June 19, 2000
	A14	THE PC GUIDE website, <i>Non-Parity, Parity and ECC Memory</i> , Site Version: 2.2.0 – Version Date: April 17, 2001; <a href="http://www.pcguide.com/ref/ram/errParity-c.html">http://www.pcguide.com/ref/ram/errParity-c.html</a>
	A15	Robert Morelos-Zaragoza, <i>The Error Correcting Codes (EEC) Page</i> , 1996-9.
	A16	Minagawa et al., <i>Pre-decoding Mechanism for Superscalar Architecture</i> , IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, May 9-10, 1991.
	A18	International Search Report for PCT/US02/12768, mailed 8/14/02

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.